

What is Claimed is:

- 1 1. A semiconductor memory, comprising:
2 a plurality of memory cells, the memory cells being connected to first lines and to
3 second lines, the second lines crossing the first lines, each memory cell having storage
4 capacitor and a selection transistor, the memory cells form at least one memory cell array,
5 wherein the first lines run divergently with respect to one another, the second lines are
6 curved, a memory cell is connected at each crossing point between a first line and a second
7 line, each of the first lines having memory cells connected thereon, the respective storage
8 capacitor being laterally offset alternately on each side of the respective first line.

- 1 2. The semiconductor memory as claimed in claim 1, wherein the first lines extend
2 divergently from a logic area to the memory cells in at least one memory cell array.

- 1 3. The semiconductor memory as claimed in claim 1, wherein the memory cells form
2 at least one memory cell array, at the memory cell array having the form of an annular
3 portion, the first lines diverging radially, and the second lines curving arcuately.

- 1 4. The semiconductor memory as claimed in claim 1, wherein one or more memory
2 cell arrays surround a logic area annularly.

- 1 5. The semiconductor memory as claimed in claim 1, wherein the first lines are bit
2 lines and the second lines are word lines.

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1 6. The semiconductor memory as claimed in claim 1, wherein the first lines are word
2 lines and the second lines are bit lines.

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1 7. The semiconductor memory as claimed in claim 1, wherein two memory cells are
2 connected to two mutually adjacent bit lines, the two memory cells being connected to the
3 same word line, the two memory cells having respective storage capacitors adjacent to one
4 another along the same word line, the two memory cells being connected to two mutually
5 adjacent bit lines.

1 8. The semiconductor memory as claimed in claim 1, wherein the storage capacitors
2 are trench capacitors buried in a semiconductor substrate.

1 9. The semiconductor memory as claimed in claim 8, wherein at least one further
2 logic area is provided on the semiconductor substrate and is arranged between a memory area
3 and an edge of the semiconductor substrate the further logic area not surrounded by memory
4 areas.

1 10. The semiconductor memory as claimed in claim 1, wherein the selection
2 transistors are vertical field effect transistors whose gate electrodes are connected to the word
3 lines.

1 11. The semiconductor memory as claimed in claim 10, wherein at least one further
2 logic area is provided on the semiconductor substrate and is arranged between a memory area

3 and an edge of the semiconductor substrate the further logic area not surrounded by memory
4 areas.

1 12. The semiconductor memory as claimed in claim 1, wherein the semiconductor
2 memory is a dynamic read/write memory.

1 13. A semiconductor memory, comprising:
2 a plurality of memory cells, the memory cells being connected to first lines and to
3 second lines, the second lines crossing the first lines, each memory cell having a storage
4 capacitor and a selection transistor, the memory cells forming at least one memory cell array,
5 wherein the first lines run divergently with respect to one another, the second lines are
6 curved, a memory cell is connected at each crossing point between a first line and a second
7 line, each of the second lines having memory cells being connected thereon, the respective
8 storage capacitor being laterally offset alternately on each side of the respective second line.

1 14. The semiconductor memory as claimed in claim 13, wherein the first lines extend
2 divergently from a logic area to the memory cells in at least one memory cell array.

1 15. The semiconductor memory as claimed in claim 13, wherein the memory cells
2 form at least one memory cell array, the memory cell array having the form of an annular
3 portion, the first lines diverging radially, and the second lines curving arcuately.

1 16. The semiconductor memory as claimed in claim 13, wherein one or more
2 memory cell arrays surround a logic area annularly.

1 17. The semiconductor memory as claimed in claim 13, wherein the first lines are bit
2 lines and the second lines are word lines.

1 18. The semiconductor memory as claimed in claim 13, wherein the first lines are
2 word lines and the second lines are bit lines.

1 19. The semiconductor memory as claimed in claim 13, wherein two memory cells
2 are connected to two mutually adjacent bit lines, the two memory cells being connected to
3 the same word line, the two memory cells having respective storage capacitors adjacent to
4 one another along the same word line, the two memory cells being connected to two mutually
5 adjacent bit lines.

1 20. The semiconductor memory as claimed in claim 13, wherein the storage
2 capacitors are trench capacitors buried in a semiconductor substrate.

1 21. The semiconductor memory as claimed in claim 20, wherein at least one further
2 logic area is provided on the semiconductor substrate and is arranged between a memory area
3 and an edge of the semiconductor substrate the further logic area not being surrounded by
4 memory areas.

5 22. The semiconductor memory as claimed in claim 13, wherein the selection
6 transistors are vertical field effect transistors whose gate electrodes are connected to the word
7 lines.

1 23. The semiconductor memory as claimed in claim 22, wherein at least one
2 further logic area is provided on the semiconductor substrate and is arranged between a
3 memory area and an edge of the semiconductor substrate the further logic area not being
4 surrounded by memory areas.

1 24. The semiconductor memory as claimed in claim 12, wherein the
2 semiconductor memory is a dynamic read/write memory.